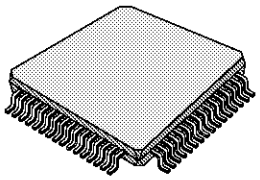
SGS-THOMSON MICROELECTRONICS

STH221

MULDEX IC FOR MULTIMEDIA TELESERVICES

- HCMOS SEA OF GATE TECHNOLOGY
- 64 PINS QUAD FLAT PACKAGE
- TWO MODES OF OPERATION: STAND-ALONE, MICROPROCESSOR
- INTERFACE FOR 8/16/32 BIT MICROPROCESSORS
- TRANSMITTER FUNCTIONS:
  Implementation of two electrical interfaces:
  - 64kbit/s only
  - to 4 up to 32 Time Slot Multiplex.
  Allocation of the multimedia frame structure in B channel for 32B channels.
  3 input internal multiplexer can multiplex up to 3 sources within the 64kbit/s output stream.
  Serial/Parallel input to the AC data:
  - Serial: using the 8th bit of the input stream.
  - Parallel: using bytes provided by microprocessor.
  Serial/parallel input for the seven sub-channels.
- RECEIVER FUNCTIONS:
  Implementation of two electrical interfaces:
  - 64kbit/s only
  - to 4 up to 32 Time Slot Multiplex
  Allocation of the multimedia frame structure in Bchannel of 32 channels.
  3 Output internal demultiplexer can demultiplex up 3 signals provided by the 64kbit/s input stream.
  Serial/parallel output for AC data:
  - Serial: using the 8th bit of the output stream.
  - Parallel: using bytes provided by microprocessor.
  Serial/parallel output for the seven subchannels.
- OTHER GENERAL ASPECTS:
  Interrupt procedures to access 16 input registers and 10 output registers.
  Working with/without external byte synchronization depending on Protocol Select Pin and bit programmation.
  The emitter and receiver provide superframe synchronization.
  Error correction on BAS (up to two consecutive errors can be corrected, three are detected).
  Fast receiver synchronization (parallel method).



PQFP64

ORDERING NUMBER: STH221

DESCRIPTION

The H221/Muldex integrated circuit is a multiplex/demultiplex for a frame structure with 8-bit data channel. Manufactured using HCMOS "Sea of gates" technology, the device requires a single 5 V supply and is available in a 64 pin Quad Flat Package. The H221/Muldex implements the frame structure for a 64 kbit/s channel in audiovisual teleservices as defined by CCITT in the H.221 recommendation with automatic generation/decoding of FAW and error correction detection on BAS. It also implements the CRC4 algorithm for error detection on the sub-multiframe structure and allows the possibility of serial and/or parallel input/output of data channels (including the AC channel). In addition the multiframe structure is supported with automatic generation/decoding of the Multiframe Alignment Word and enabling of multiframe count. The H221/Muldex is controlled by a microprocessor using an 8-bit data bus or can function in a stand-alone mode; standard 64 kbit/s or time division multiplex interface are implemented.

PIN CONNECTION (Top view)

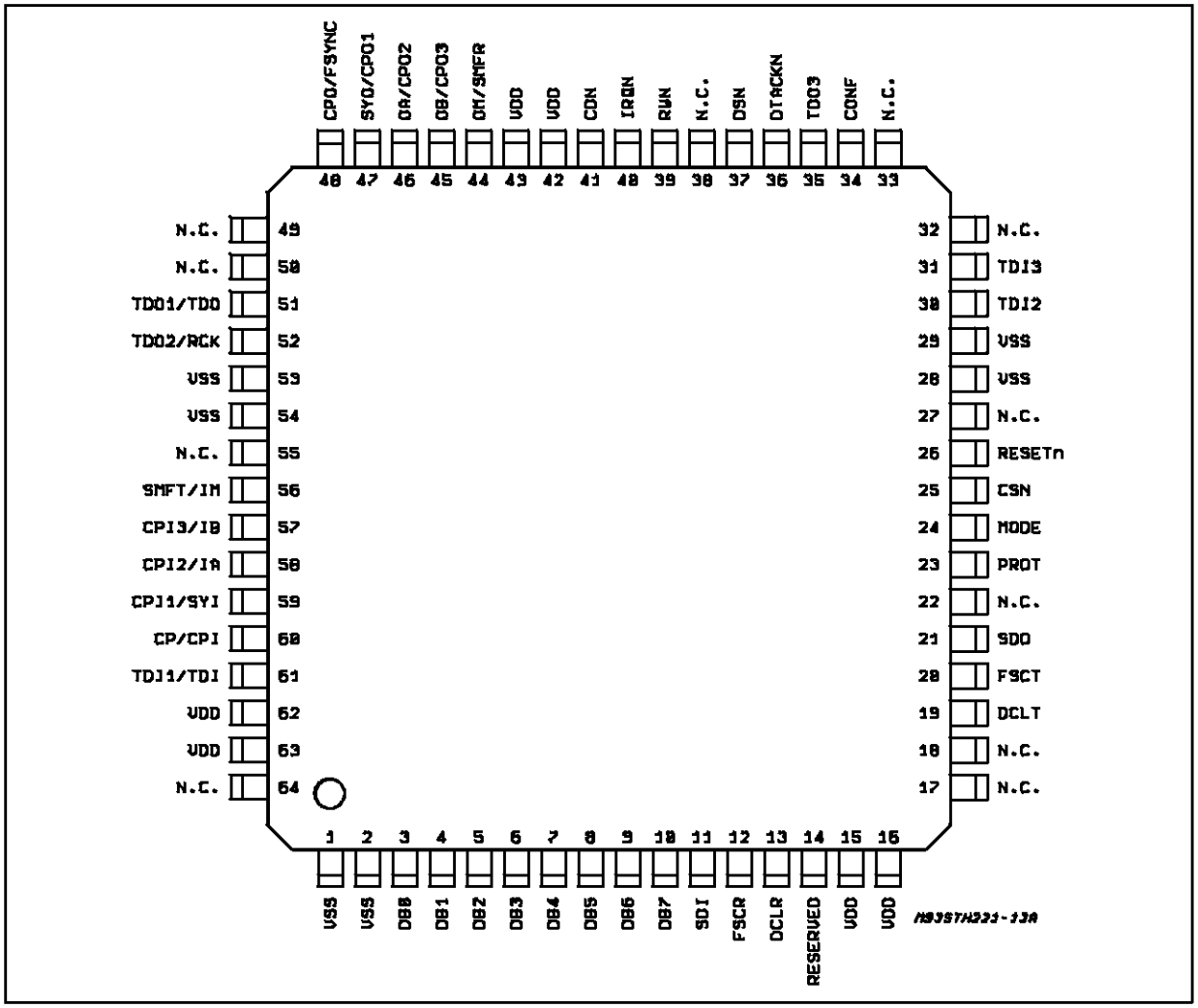


Table 1: Alphabetical Listing of Symbols.

Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin
CDN	41	DB0	3	SMFR/OM	44	VSS	1,2,28,29,53, 54
CONF	34	DB1	4	FSCR	12	SMFT/IM	56
CP/CPI	60	DB2	5	FSCT	20	TDI1/TDI	61
CPI1/SYI	59	DB3	6	FSYN/CPO	48	TDI2	30
CPI2/IA	58	DB4	7	IRQN	40	TDI3	31
CPI3/IB	57	DB5	8	MODE/TEST	24	TDO1/TDO	51
CPO1/SYO	47	DB6	9	PROT	23	TDO2/RCK	52
CP02/OA	46	DB7	10	RESETN	26	TD03	35
CP03/OB	45	DCLR	13	RWN	39	VDD	15,16,42,43, 62,63
DSN	37	DCLT	19	SDI	11	CSN	25
DTACKN	36	SDO	21				

Pin 16 must not be connected.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
3-10	DB0-DB7	I/O	CPU	**I/O Data µP Interface.**
11	SDI	I	Rx	**Serial Data Input**. Input of serial stream from line into the receiver. 64 kbit/s or 256 kbit/s up to 2048kb/sec (GCI).
12	FSCR	I	Rx	**Frame Syncro Rx.** Octet synchronization (if present) for the receiver.
13	DCLR	I	Rx	**Data Clock Rx.** Clock of input data for receiver. 64 khz or 512 up to 4096 khz (GCI)
19	DCLT	I	Tx	**Data Clock Tx.** Clock of output data from transmitter. 64 khz or 512 up to 4096 khz (GCI)
20	FSCT	I	Tx	**Frame Syncro Tx.** Octet syncronization (if present) for the transmitter.
21	SDO	O*	Tx	**Serial Data Output**. Output of serial stream from transmitter into B channel selected. Open drain in GCI mode.
23	PROT	I		**Protocol select**. Select of protocol implementation: 0 = 64 kbit/s 1 = Multiplex at 512 up to 2048kb/s.
24	MODE/ TEST	I		CONF = 1 Test is given by this pin. Specific test mode of the component. In normal operation, must be 0. CONF = 0. Selection of working mode. MODE = 0. Controlled by CPU (CPU mode) MODE = 1. Stand Alone (S-A Mode). mode). Test is given by Bit 3 of Command Register.
25	CSN	I	CPU	**Chip Select.** In CPU mode allows the selection of the component by the CPU: 0 = The CPU can access internal registers using RWN, CDN, DSN signals. 1 = The H221 is disabled. In S-A mode this pin represents the N5 bit of the H221 protocol (Enable/disable of the multiframe count).
26	RESETN	I		**Reset component**. Reset the H221 and initializes default conditions. Low Signal = active Minimum duration = 1µs.
30	TDI 2	I	Tx	**Terminal Data Input 2.** Serial input of data for the transmitter, clocked by CP. Data is shifted on the falling edge of CP. Usable only if CONF = 1 otherwise ignored.
31	TDI 3	I	Tx	**Terminal Data Input 3.** Serial input of data for the transmitter. Data is shifted on the falling edge of CP. Usable only if CONF = 1 otherwise ignored.
34	CONF	I		**Configuration.** CONF = 0. CPI, TDI, SYI, IA, IB, IM, OM, TDO, CPO, SYO, OA, OB, RCK, Mode pins are validated. CONF = 1. CP, TDI 1/3, CPI 1/3, TDO 1/3, CPO 1/3, SMFT, SMFR, TEST, FSYN pins are validated.
35	TDO 3	O	Tx	**Terminal Data Output 3.** Serial Output of data received. Data is shifted on the rising edge of CP. If CONF = 1: Open Drain else TDO3 = 0.
36	DTCAKN	O	CPU	**Data Acknowledge**. Data acknowledge for writing from CPU and data ready for reading. 1 = Data not yet ready or acknowledged. 0 = Data ready or acknowledged. In S-A mode it represents the Aloc signal.
37	DSN	I	CPU	**Data Strobe**. Strobe signal for data I/O from/to CPU. 0 = Data Valid on data bus. In S-A mode it is used to strobe the BAS data on the data bus.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
39	RWN	I	CPU	**Read or Write**. Indicates whether the next data transfer performed is a read or a write. 0 = Write operation. 1 = Read operation. In S-A mode it indicates the direction of the BAS data on data bus.
40	IRQN	OD	CPU	**Interrupt Request.** When low indicates that the H221 is requesting interrupt service. This lead goes high when the CPU performs the interrupt acknowledge. It is an open drain so pull-up resistor is needed. In S-A mode it represents the Eloc signal.
41	CDN	I	CPU	**Command or Data**. Selection between the command register or the data registers set. 0 = The CPU accesses a data register. 1 = The CPU accesses the command register. In S-A mode it enables the computing of the CRC4 value by the transmitter. 0 = Tx computers CRC4 value. 1 = All 1's are transmitted on the CRC4 position (CRC4 disabled).
44	SMFR/ OM	O	Rx	CONF = 1. Submultiframe received. This signal goes high at the beginning of first bit of octet 1 of every submultiframe. It returns low at the beginning of first bit of octet 83 of every submultiframe. CONF = 0 Out Mask. Frame synchronization; it goes high before the beginning of first bit of octet 1 of every frame. It returns low between the 16th and the 72nd octet, depending on the programmed conditions. Valid only when the receiver is frame aligned.
45	CP03/ OB	O	Rx	CONF = 1. Clock pulse for data output 3. This signal is configurated by CPS and WIN bits. It is associated to TDO3 data. CONF = 0. Out multiplex addr. B. LSB of the channel number of the bit on the TDO output.
46	CP02/ OA	O	Rx	CONF = 1. Clock pulse for data output 2. This signal is configurated by CPS and WIN bits. It is associated to TDO2 data. CONF = 0. Out multiplex addr. A. Together with OA and SYO indicates the channel number of the bit on the TDO output. These signals can be used to address an external demultiplexer separating 8 sub-channels.
47	SYO/ CPO1	O	Rx	CONF = 1. Clock pulse for data output 1. This signal is configurated by CPS and WIN bits. It is associated to TD01 data. CONF = 0. Synchro Output MSB of the channel number of the bit on the TDO output. It also represents the synchronization octet; SYO is low at the beginning of the octet.
48	FSYN/ CPO	I	-	CONF = 1. Frame Synchronization. This 8kHz signal indicates the first bit of the first time slot for TDO1, TDO2, TDO3, TDI1, TDI2, TDI3 multiplex. CONF = 0 Clock Pulse Output; Clock for the output of data from receiver. The clock input must have a mimimum frequency of 64 KHz and a maximum frequency of 2 MHz. Signals OA, OB and SYO have meaning only whne CPO has a 64 KHz frequency.

Table 2: Pin Description.

Pin	Symbol	Mode	Type	Function
51	TDO1/ TDO	TS/O	Rx	CONF = 1. Terminal Output 1. Serial output of data received. Data is shifted on the rising edge of CP. OPEN DRAIN CONF = 0. Terminal Data Output. Serial output of data received, clocked by CPO. Data is shifted on the leading edge of CPO.
52	TDO2/ RCK	TS/O	Rx	CONF = 1. Terminal Output 2. Serial output of data received. Data is shifted on the rising edge of CP. OPEN DRAIN CONF = 0. Rx Clock. A 64 KHz clock recovered by the receiver from the incoming stream.
56	SMFT/ IM	0	Tx	CONF = 1. Submultiframe transmitted. This signal goes high at the beginning of first bit of octet 1 of every submultiframe. It returns low at the beginning of first bit of octet 8 of every submultiframe. CONF = 0. Input Mask. Input Mas. Frame synch; it goes high before the transmission of the first bit of octet # 1 of every frame. It returns low between the 16th and the 72nd octet, depending on the programmed conditions.
57	CPI3/ IB	0	Tx	CONF = 1. Clock Pulse for data input 3. This signal is configurated by CPS and WIN bits. It is associated to TDI3 data. CONF = 0. Input Mask. In multiplex addr. B. LSB of the channel number of the bit on the TDI input.
58	CPI2/ IA	0	Tx	CONF = 1. Clock Pulse for data Input 2. This signal is configurated by CPS and WIN bits. It is associated to TDI2 data. CONF = 0. In Multiplex Addr. A In multiplex addr. A. Together with IA and SYI indicates the channel number of the bit on the TDI input. These signals can be used to address the multiplexing of 8 sub-channels.
59	CPI/ SYI	O	Tx	CONF = 1. Clock Pulse for data input 1. This signal is configurated by CPS and WIN bits. It is associated to TDI1 data. CONF = 0. Input Synchronization .Input Sync. MSB of the channel number of the bit on the TDI input. It also represents the sync of the outgoing octet i.e. SYI is low at the beginning of the octet.
60	CP/CPI	I	Tx-Rx/ Tx	CONF = 1. Clock Pulse. This signal is used to generate six clock pulses: CPI1, CPI2, CPI3 and CPO1, CPO2, CPO3. Its frequency is twice binary data rate of TDI1, TDI2, TDB and TDO1, TDO2, TDO3 multiplex. Minimum frequency 128kHz. Maximum frequency 4096kHz. CONF = 0. Clock Pulse input. Clock for the input of data into transmitter. The clock input must have a minimum frequency of 64kHz and a maximum frequency of 2 MHz. Signals IA, IB and SYI have meaning only when CPI has a 64kHz frequency.
61	TDI1/ TDI	I	Tx	CONF = 1. Terminal Data Input 1. Serial input of data for the transmitter. Data is shifted on the falling edge of CP. CONF = 0. Terminal Data Input. Serial input of data for the transmitter, clocked by CPI. Data is shifted on the leading edge of CPI.

OVERVIEW

The H221/Muldex performs complete multiplexing/demultiplexing according to the CCITT H.221 recommendation. It generates and decodes frame and multiframe structure automatically without intervention by the host CPU. The host CPU must initialize the H221 registers and supply or read BAS and AC information upon request. The CPU is notified of important events via interrupt. The H221/Muldex contains a receiver, a transmitter and an interface unit (fig. 1).

ARCHITECTURE

Transmitter

The transmitter can work in two main modes: unframed or framed. In the first mode, octets to be transmitted are shifted out on the serial data output (SDO) without any data insertion or control; in framed mode, the transmitter constructs the frame, submultiframe and multiframe structure. Data is shifted on the rising edge of the data clock signal (DCLT).

In framed mode the transmitter handles bit # 8 of the octets: it puts into octets 1 to 16 information that identifies the frame structure (FAW, BAS, Parity, CRC4, A, E, according to the submultiframe); into octets 17 to 80 the transmitter puts the AC channel information.
This data can be sent to the AC register of the transmitter by the host CPU or can be the 8th bit of the incoming bit stream, depending on the configuration set by CPU. A request for AC data is made by the CPU via interrupt; the transmitter generates an interrupt request 1mS before it needs the data. After this time it transfers the AC data into internal register and starts the transmission of the next 8 octets. Then the cycle restarts with another interrupt request.

The same mechanism is applied to the BAS data request; SMFT pin generates a signal every 20ms.

This submultiframe transmit signal is at ”1”during FAS transmitting. CPU can update if necessary BAS data and configuration registers TDI1R, TDI2R, TDI3R, when SMT is low. BAS data will be emitted during the next submultiframe and the new configuration of TDI1, TDI2, TDI3 multiplex will be actual after this next submultiframe. If not updated, old data is emitted.

The transmitter puts into the first bit of every information that identifies the multiframe structure; some are fixed and generated by the transmitter (MAW), others are variable (multiframe counter, L1, L2, L3, R bits and TEA). When enabled, the multiframe count is generated automatically by the transmitter, if disabled, all zeroes are transmitted; other bits are sent by the host CPU into the TFAS register. This data is transferred into internal register for transmission at the beginning of a multiframe (i.e. on the first bit of the frame # 0); if necessary data can be updated by the CPU before the end of a multiframe; no interrupt request is generated for this data.

The transmitter also computes the CRC4 value of a submultiframe and puts this value on the next odd frame according to the CCITT H221 recommendation; at reset, for the first two frames a zero value is transmitted; if the CRC4 computing is not enabled, the transmitter sends all ones in the CRC4 position.

Receiver

The receiver, like the transmitter, has two working modes: unframed and framed. In the first mode, octets received into the serial input (SDI) are shifted out on the terminal data (TDO) without any control or synchronism search; in framed mode, the receiver detects frame and multiframe alignment words (FAW and MAW) following procedures specified in CCITT H221 recommendation.
When frame alignment is obtained, the receiver computes parity for BAS data; it uses this data for correcting up to two errors on BAS; 3 errors are detected.

If aligned, the receiver also decodes AC data; the availability of the data is signalled to the host CPU via interrupt; the CPU has 1ms to remove the data before the AC register is updated with the new value. The AC data is also available as the 8th bit of octets on terminal data output (TDO) when the component is receiving octets 17 to 80. The number of interrupt generated for the AC channel depends on the configuration set by CPU.

BAS register (RBAS) is updated every submultiframe when receiving octet 17 of the odd frame (i.e. after the parity has been verified); CPU can read BAS data when SMFR is low. SMFR pin generates a signal every 20ms. This Submultiframe Receive Signal is at ”1”during an even frame and FAS and BAS receiving of odd frame. After reading BAS data, CPU can load immediately into TDO1R, TDO2R, TDO3R register when SMFR is yet low to change the configuration of TDO1, TDO2, TDO3 multiplex if necessary. Errors detected on BAS data (corrected or not) are signalled to the host CPU via interrupt; reading the receiver status register the CPU can determine the type of error.

The data on the BAS register is not valid if errors on BAS are not recoverable. In the first bit of every frame the receiver reads information concerning multiframe structure; registers that hold this information (multiframe counter (RC), L1, L2, L3, R bits and TEA (RFAS)) are updated at the beginning of a multiframe; the CPU can read multiframe data at any time except on the first octet of the first frame of a multiframe.

The receiver also computes the CRC4 value of a submultiframe and compares it with the received value of CRC4; if discrepancies are found, bit Eloc is set and an interrupt is generated; error interrupts are generated at the beginning of a frame only when some error condition are present.

Interface

The interface unit provides interface between the host CPU and the H221 Muldex transmitter and receiver via data bus and some control signals. The interface holds general purpose register and decoding logic for the addressing of transmitter and receiver registers. Using data-strobe/data-acknowledge protocol, the H221/Muldex can interface CPU that use synchronous or asynchronous read/write cycles.

PRINCIPLES OF OPERATION

CPU Interface

The CPU has direct access into two register, command or data, using the CDN signal. The data register is split in 16 registers; the address of the data register is specified in the command register. The CPU configures the H221/Muldex by writing the command and data registers. Status information can be accessed by reading one of the status registers and is used to monitor the H221/Muldex operation. The most useful information is coded in the command/status register for fast access by the CPU.

H221 Registers

The H221/Muldex registers are divided into four classes: command/status, receiver, transmitter, test.

Command/Status Register. Direct access by CPU when CDN signal is high; contains interrupt and error flags, controls the addressing of data registers, the clearing of interrupt flags, the test mode and the start of the transmitter.

Receiver Registers. These registers contain information received: multiframe data, BAS data, AC data, octet. Other registers contain status information of the receiver: frame and multiframe counters, AC counter, status bit indicating level of synchronization achieved (octet, frame, multiframe).

Transmitter Registers. These registers contain information to be transmitted: multiframe data, BAS data, AC data, octect. Other registers contain status information of the transmitter: frame and multiframe counters, AC counter, bits programming the operating mode of the transmitter.

Test Register. These registers contain data used for the testing of the component; not used in normal operation.

Table 3: Common/Status Register Definition.

Bit	7	6	5	4	3	2	1	0
(Write) Field	IR	IT	IE	S	W3/T	W2	W1	W0

Bit	Symbol	Name/Description
0	W0	**Data Register Address** (bit 0). Interpreted with W1 (bit 1) and W2 (bit 2) and W3 [(bit 3) + if CONF = 1] as the address of the data register as indicated by the following table:

W3	W2	W1	W0	Write	Read
0	0	0	0	TFAS	RFAS
0	0	0	1	TBAS	RBAS
0	0	1	0	TAC	RAC
0	0	1	1	TEST	TC
0	1	0	0	TEST	RC
0	1	0	1	COND	RXST
0	1	1	0	ACS/TEST	RTACC
0	1	1	1	TPD	RPD
Available only if CONF = 1					
1	0	0	0	TSAA	TBCR
1	0	0	1	TDO1R	-
1	0	1	0	TDO2R	-
1	0	1	1	TDO3R	-
1	1	0	0	TSAN	RBCR
1	1	0	1	TDI1R	-
1	1	1	0	TDI2R	-
1	1	1	1	TDI3R	-

Forced to 1 if MODE pin is high and CONF = 0.

1	W1	**Data Register Address** (bit 1). Forced to 0 when MODE pin is high and CONF = 0.
2	W2	**Data Register Address** (bit 2). Forced to 0 when MODE pin is high and CONF = 0.
3	W3/T	**Data Register Address** (bit 3) if CONF = 1. **CR Test if CONF = 0.** Specifies test mode of the component. In normal operation must be 0. T is cleared by hardware reset or by software reset (bit RSN of COND register). If CONF = 1, this function is performed through pin MODE/TEST
4	S	**Start/Interrupt Enable**. When this bit goes high, the transmitter starts transmitting the first bit of the first frame of a multiframe. If it remains high, generation of all interrupts is enabled. If it returns low interrupts are disabled. Two consecutive writes to this bit (1-0) are sufficient to start the transmitter. The transmitter starts on the second falling edge of SYI signal (fig. 5). S is cleared by hardware reset or by software reset (bit RSN of COND register).
5	IE	**Error Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.
6	IT	**Transmitter Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.
7	IR	**Receiver Interrupt Acknowledge**. Writing 1 on this bit clears the corresponding interrupt flag.

Table 3: Common/Status Register Definition. (Continued)

Bit	7	6	5	4	3	2	1	0
(Read) Field	IR	IT	IE	ELOC	ALOC	EBC	EB	0

Bit	Symbol	Name/Description
0	–	**Unused bit**. Read always as zero.
1	EB	**BAS Data Error** When 1 indicates an unrecoverable error on the BAS data. This bit is updated on a submultiframe basis.
2	EBC	**BAS Data Error Recovered** When 1 indicates that BAS data has been received with an or 2 errors and that error has been corrected by the error correction logic.
3	ALOC	**Local Alignment**. When 0 indicates that the receiver is aligned on frame and multiframe. The same bit is transmitted as bit A of the frame if ASEL bit of ACS/TEST register allows it.
4	ELOC	**Local Error**. When 1 indicates a difference between the CRC4 value calculated by the receiver and the CRC4 received. The same bit can be transmitted as bit E of the frame
5	IE	**Error Interrupt Flag.** When 1 indicates that an error interrupt has been generated by the component. It returns 0 on error interrupt acknowledge.
6	IT	**Transmitter Interrupt Flag**. When 1 indicates that a transmitter interrupt has been generated by the component. It returns 0 on transmitter interrupts acknowledge.
7	IR	**Receiver Interrupt Flag.** When 1 indicates that a receiver interrupt has been generated by the component. It returns 0 on receiver interrupt acknowledge.

Table 4: TFAS Register Definition (Address 0000).

Bit	7	6	5	4	3	2	1	0
(Write) Field	EPI	SYNEXT	N5	TEA	R	L3	L2	L1
Hardware RESET configuration	0	1	X	0	0	0	0	0

Bit	Symbol	Name/Description
0-3	L1-L3, R	**L1-L3, R bits.** L1-L3 and R bits of H221 multiframe structure. Cleared by hardware or software reset.
4	TEA	**TEA bit**. Terminal Equipment Alarm bit to be transmitted. Cleared by hardware or software reset.
5	N5	**N5 bit**. Multiframe count enable. When 1 the transmitter counts multiframe sending multiframe number in descending order on bit N1N4 (N1 = LSB). No default on reset.
6	SYNEXT	**Transmitter Octet Syncro Valid.** Specifies if external octet synchro is valid. If 1, the external octect syncro is present and valid; if 0, the octet synchro may be present but it is not taken into account by transmitter. Hardware or software reset forces this bit to 1.
7	EPI	**Enable Parallel Input**. When 1 enables parallel input of data to be transmitted using TPD register. If this bit is 0 data enters serially through the TDI input. Cleared by hardware or software reset.

Table 5: RFAS Register Definition (Address 0000).

Bit	7	6	5	4	3	2	1	0
(Read) Field	0	0	N5	TEA	R	L3	L2	L1

Bit	Symbol	Name/Description
0-3	L1-L3, R	**L1-L3, R bits.** L1-L3 and R bits of H221 multiframe structure.
4	TEA	**TEA bit**. Terminal Equipment Alarm bit received.
5	N5	**N5 bit**. Enable multiframe count bit received. If 1 the remote transmitter has multiframe numbering enabled.
6-7	–	**Unused bits**. Read as zero.

Table 6: TBAS and RBAS Register Definition (Address 0001).

Bit	7	6	5	4	3	2	1	0
Field	b_0	b_1	b_2	b_3	b_4	b_5	b_6	b_7

Bit	Symbol	Name/Description
0-7	b_0b_7	**BAS Data**. BAS data to be transmitted (TBAS Register write) or received (RBAS Register read). b_0 is the MSB and b_7 the LSB as defined by CCITT.

Rem: Hardware RESET is inactive on configuration.

Table 7: TAC and RAC Register Definition (Address 0010).

Bit	7	6	5	4	3	2	1	0
Field	AC_7	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0

Bit	Symbol	Name/Description
0-7	AC_0AC_7	**AC Data**. AC data to be transmitted (TAC Register write) or received (RAC Register read). In TAC register AC_0 is the first bit transmitted while in RAC register AC_0 represents the last bit received.

Rem: Hardware RESET is inactive on configuration.

Table 8: TC Register Definition (Address 0011).

Bit	7	6	5	4	3	2	1	0
(Read) Field	TN_4	TN_3	TN_2	TN_1	TF_3	TF_2	TF_1	TF_0

Bit	Symbol	Name/Description
0-3	TF_0TF_3	**Transmitter Frame Counter**. Indicates the frame number in transmission (i.e. the frame position within the multiframe structure). TF_0 is the LSB.
4-7	TN_1TN_4	**Transmitter Multiframe Counter**. Indicates multiframe number in transmission and represents bit N1N4 of the multiframe structure. TN_1 is the LSB.

Rem: Write register used for TEST only
: No access to user

Table 9: RC Register Definition (Address 0100).

Bit	7	6	5	4	3	2	1	0
(Read) Field	RN_4	RN_3	RN_2	RN_1	RF_3	RF_2	RF_1	RF_0

Bit	Symbol	Name/Description
0-3	RF_0RF_3	**Receiver Frame Counter**. Indicates the receiving frame number (i.e. the frame position within the multiframe structure). RF_0 is the LSB.
4-7	RN_1RN_4	**Receiver Multiframe Counter**. Indicates bit N1 N4 of the received multiframe structure. RN_1 is the LSB.

Rem: WRITE register used for TEST only
: No access to user.

Table 10: COND Register Definition (Address 0101).

Bit	7	6	5	4	3	2	1	0
(Write) Field	ENEL	ENCRC	SYNEXR	RSN	ACS	N5IEN	B1B2N	FUN
Hardware RESET Configuration	1	0	0	1	1	1	1	1

Bit	Symbol	Name/Description
0	FUN	**Framed or Unframed Mode**. Specifies if the transmitter generates frame and multiframe structure. If 1 the transmitter sends FAS, BAS, AC, CRC4, A, E and multiframe information on bit 8 of transmitting data. If 0 the 8th bit is passed as is from TDI input to SDO output. Hardware reset forces this bit to 1.
1	B1B2N	**B1 or B2 Position**. When GCI mode active and CONF set to 0, specifies the position of the octet on the input or output data stream. If 1 the octet is placed on B1 position; if 0 on B2 position. In 64 kbit/s mode or CONF set to 1, B1B2N has no meaning. Hardware reset forces this bit to 1. When CONF is set to 1, the desired position is defined through bits 4 to 0 of TSAN register (TSN4, TSN3, TSN2, TSN1, TSN0).
2	N5IEN	**N5 Internal or External**. Specifies the source of N5 bit (multiframe count enable). If 1 the N5 bit of the transmitter is the complement of the Aloc bit of the receiver. In this case the transmitter starts multiframe count automatically when the receiver is aligned. If N5IEN = 0, the N5 bit of the transmitter is the bit contained in the TFAS register. In this case the transmitter starts multiframe count when the CPU writes 1 on N5 bit of TFAS register. Hardware reset forces this bit to 1.
3	ACS	**AC Mode Select**. Specifies the way AC data is exchanged with the terminal: parallel or mixed mode (serial/parallel). If 0, AC data are sent to H221/Muldex by CPU through data bus 8 bits at a time (parallel mode) upon interrupt request. Eight interrupt requests are generated by the transmitter at the beginning of octets 9, 17, 25, 33, 41, 49, 57, 65; the CPU has 1mS to update the AC register (TAC), then the 8 bits of AC are transmitted (for data requested on octet 9 the transmission starts at octet 16 and ends at octect 24, AC0 bit first). Eight interrupt requests are generated by the receiver at the beginning of octets 25, 33, 41, 49, 57, 65, 73, 1; the CPU has 1ms to remove data from AC register (RAC), then the AC register is updated with the new received data (in octet 25 is presented data received in octets 16 to 24, AC0 bit first). If the ACS bit is 1, AC data are sent to H221/Muldex in a mixed mode (parallel/serie). Parallel data are requested first; the number of parallel AC data is specified on bits $ACSE_0$ $ACSE_2$ of ACS/TEST register. The remaining part of the AC data is sent to the transmitter as the 8th bit of the stream coming into the TDI pin. Interrupt request is generated only for parallel data. The receiver gives AC data simultaneously in both ways but generates interrupt request only for parallel data. Hardware reset forces this bit to 1.

Table 10: COND Register Definition (Continued).

Bit	Symbol	Name/Description
4	RSN	**Reset Software**. When 0, this bit forces reset state of the component and initializes default conditions in all registers except the COND register itself. Hardware reset forces this bit to 1.
5	SYNEXR	**Receiver Octet Syncro Valid**. Specifies if external octet synchro is valid. If 1, the external octet synchro is present and valid; if 0, the octet synchro may be present but it is not taken into consideration by the receiver. Hardware reset forces this bit to 0.
6	ENCRC	**Enable CRC4 Calculation**. Specifies whether the transmitter has to calculate and transmit the value of CRC4. If 1, the transmitter calculates and transmits the CRC4 value; if 0, the value of CRC4 is not calculated and all ones are transmitted on the CRC4 position. Hardware reset forces this bit to 0.
7	ENEL	**Enable transmission of Eloc.** Specifies is the Eloc signal is passed from the receiver to the transmitter. If 1, the receiver passes the Eloc bit (the result of comparison between CRC4 received and calculated) to the transmitter. If 0, no value is transferred and the transmitter always sends 0 on the E bit position. Hardware reset forces this bit to 1.

Table 11: RXST Register Definition (Address 0101).

Bit	7	6	5	4	3	2	1	0
(Read) Field	CRCA1	–	–	SM	SF	SO	E	A

Bit	Symbol	Name/Description
0	A	**Alignment Loss**. When 1 indicates a loss of alignment in the remote receiver. It represents the A bit received in odd frames.
1	E	**CRC4 Error**. When 1 indicates an error on the CRC4 computing by the remote receiver. It re presents the E bit received in odd frames.
2	SO	**Octet Synchronization**. When 1 indicates that the receiver has achieved octet synchronization by recognizing the FAS position on the frame structure.
3	SF	**Frame Synchronization**. This bit goes high when the receiver validates the received frame as specified by CCITT H221 rec. It remains high until a loss of frame alignment is recognized.
4	SM	**Multiframe Synchronization**. This bit goes high when multiframe alignment is achieved by the receiver that recognizes the multiframe alignment signal. It returns low when three consecutive multiframe alignment signals have been received with an error.
5-6	–	**Unused bits**. Read undefined.
7	CRCA1	**CRC4 All Ones**. When 1 indicates that the received CRC4 data contains all ones. This can be a symptom that indicates the disabling of the CRC4 calculation by the remote transmitter.

Table 12: ACS/TEST Register Definition (Address 0110).

Bit	7	6	5	4	3	2	1	0
(Write) Field	$ACSE_2$	$ACSE_1$	$ACSE_0$	RRES	ASEL	AEXT	RSBT	RCL
Hardware RESET Configuration	0	0	0	0	0	X	0	X

Bit	Symbol	Name/Description
0	RCL	**Recirculate Control**. Specifies recirculating of the output stream into the receiver for local testing purposes. If 1, the output of the transmitter is internally recirculated into the receiver. The output pin (SDO) is forced to 1 when in 64 kbit/s mode (3-state when in GCI mode), the data on the input pin (SDI) is ignored. This bit has meaning only when bit T of command register is 1.
1	RSBT	**Reset bit timing**. When this bit goes high, the bit timing of the transmitter is initialized. This function may be used to synchronize two or more transmitters (fig. 6). Hardware or software reset force this bit to 0. Valid only when T bit of command register is 0; if bit T = 1 the RSBT bit should be 0.
2	AEXT	**External A bit**. Represents the value of the transmitted A bit when ASEL bit is 1. No default on hardware or software reset. Valid only when T bit of command register is 0; if bit T = 1 the AEXT bit should be 0.
3	ASEL	**A bit select**. This bit specifies the source of the A bit transmitted on odd frames. If 1 the value of A is that of the AEXT bit of this register (see below). If 0 the A bit is generated internally by the receiver and indicates the frame and multiframe alignment. Hardware or software reset force this bit to 0. Valid only when bit T of command register is 0; if bit T = 1 the ASEL bit should be 0.
4	RRES	**Receiver Restart**. Controls the restart of the receiver alignment. If 1, the receiver restarts octet, frame and multiframe alignment, regardless of the current level of alignment. Hardware reset forces this bit to 0.
5	$ACSE_0$	**AC Select**. (bit 0) Interpreted with $ACSE_1$ and $ACSE_2$ as the number of serial AC channels as indicated by the following table:
6	$ACSE_1$	**AC Select**. (bit 1). Hardware reset forces this bit to 0.
7	$ACSE_2$	**AC Select**. (bit 2). Hardware reset forces this bit to 0.

$ACSE_2$	$ACSE_1$	$ACSE_0$	IM/OM	AC#
0	0	0	16	8
0	0	1	72	1
0	1	0	64	2
0	1	1	56	3
1	0	0	48	4
1	0	1	40	5
1	1	0	32	6
1	1	1	24	7

The IM and OM signals go high at the beginning of the first octet of the frame and return low at the end of the octet indicated by the 4th column of the table. The 5th column indicates how many serial octets are input to the transmitter. When signals IM and OM are high, interrupt are generated respectively by the transmitter and the receiver; when signals return low no more interrupts are generated; in this way IM and OM signals indicate the switching between parallel and serial mode of AC channel. ACSE bits have meaning only when ACS bit of COND register is high; otherwise ACSE bit must be zero. Hardware reset forces this bit to 0.

Table 13: RTACC Register Definition (Address 0110).

Bit	7	6	5	4	3	2	1	0
(Read) Field	–	–	ACT_2	ACT_1	ACT_0	ACR_2	ACR_1	ACR_0

Bit	Symbol	Name/Description
0-2	ACR_0ACR_2	**Receiver AC Counter**. Indicates the byte number of the AC in the RAC register. E. g. when 0 indicates that RAC contains 8 bit of AC channel received in octets 17 to 24.
3-5	ACT_0ACT_2	**Transmitter AC Counter**. Indicates the byte number of the AC in the TAC register. E. g. when 0 indicates that CPU must write into TAC register AC data that will be transmitted in octets 17 to 24.
6-7	–	**Unused bits**. Read undefined.

Table 14: TPD and RPD Register Definition (Address 0111).

Bit	7	6	5	4	3	2	1	0
Field	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d0

Bit	Symbol	Name/Description
0-7	d_0d_7	**Parallel Data**. This register contains parallel data to be transmitted (TPD) or received (RPD). The TPD register is used by the transmitter only when the EPI bit of COND register is 1 and it must be updated by CPU every octet; its content is transferred on the output register on the rising edge of the clock (DCLT) that marks the beginning of the octet. THe RPD register is updated by the receiver on the first bit of the octet; CPU can read the register at any time but during the first bit of every octet. The bit d_7 is the first bit of the octet entered into the receiver and the first bit of the octet shifted out from the transmitter.

Rem: Hardware RESET is inactive on configuration.

Table 15: TSAA Register Definition (Address 1000).

Bit	7	6	5	4	3	2	1	0
(Write) Field	NM8	WIN	CPS	TSA4	TSA3	TSA2	TSA1	TSA0
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0-4	TSA0 - TSA4	Time Slot Side Application. These 5 bits indicate the time Slot selected of 32 Time Slots corresponding to 64kb/s channel for transmitting and receiving. The receiver delivers eight bits onto TD01, TD02, TD03 pins with clock pulses CP01, CP02, CP03 during the Time Slot selected.. The transmitter receives eight bits from TDI1, TDI2, TDI3 pins and delivers clock pulses CPI1 and CPI2 and CPI3 during the same Time Slot. Pulse relating to FAS and BAS is delivered if bit NM8 = 1.
5	CPS	Clock Pulse Simple. The Frequency of CPI1-3, CPO1-3 clocks and Data rate of TDI1-3, TDO1-3 are the same. CPS = 0 and WIN = 0. The frequencies of CPI1-3, CPO1-3 is twice Data rate of TDI-3, TDO1-3.
6	WIN	Window. WIN = 1. CPI 1-3 and CP0 1-3 pins deliver windows. WIN = 0. CPI 1-3 and CPO1-3 pins deliver clock pulses.
7	NM8	Non Masked bit 8. NM8 = 1. Clock pulse (or window) relating to FAS and BAS is delivered. NM8 = 0. Clock pulse (or window) relating to FAS and BAS is not delivered.

Table 16: TBCR Register Definition (Address 1000).

Bit	7	6	5	4	3	2	1	0
(Read) Field	TF0	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Bit	Symbol	Name/Description
0-6	TB0-6	Transmit Byte. This counter indicates the number of octet which is being transmitted (Modulo 80).
7	TF0	Transmit frame. TF0 = 0 Even frame. TF0 = 1 Odd frame.

Table 17: TDO1 Register Definition (Address 1001).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R81	R71	R61	R51	R41	R31	R21	R11
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R11	Subchannel 1 Received is switched on TDO1 pin.
1	R21	Subchannel 2 Received is switched on TDO1 pin.
2	R31	Subchannel 3 Received is switched on TDO1 pin.
3	R41	Subchannel 4 Received is switched on TDO1 pin.
4	R51	Subchannel 5 Received is switched on TDO1 pin.
5	R61	Subchannel 6 Received is switched on TDO1 pin.
6	R71	Subchannel 7 Received is switched on TDO1 pin.
7	R81	Subchannel 8 Received is switched on TDO1 pin.

Table 18: TD02 Register Definition (Address 1010).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R82	R72	R62	R52	R42	R32	R22	R12
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R12	Subchannel 1 Received is switched on TDO2 pin.
1	R22	Subchannel 2 Received is switched on TDO2 pin.
2	R32	Subchannel 3 Received is switched on TDO2 pin.
3	R42	Subchannel 4 Received is switched on TDO2 pin.
4	R52	Subchannel 5 Received is switched on TDO2 pin.
5	R62	Subchannel 6 Received is switched on TDO2 pin.
6	R72	Subchannel 7 Received is switched on TDO2 pin.
7	R82	Subchannel 8 Received is switched on TDO2 pin.

Table 19: TDO3 Register Definition (Address 1011).

Bit	7	6	5	4	3	2	1	0
(Write) Field	R83	R73	R63	R53	R43	R33	R23	R13
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	R13	Subchannel 1 Received is switched on TDO3 pin.
1	R23	Subchannel 2 Received is switched on TDO3 pin.
2	R33	Subchannel 3 Received is switched on TDO3 pin.
3	R43	Subchannel 4 Received is switched on TDO3 pin.
4	R53	Subchannel 5 Received is switched on TDO3 pin.
5	R63	Subchannel 6 Received is switched on TDO3 pin.
6	R73	Subchannel 7 Received is switched on TDO3 pin.
7	R83	Subchannel 8 Received is switched on TDO3 pin.

Table 20: TSAN Register Definition (Address 1100).

Bit	7	6	5	4	3	2	1	0
(Write) Field	MGN2	MGN1	MGN0	TSN4	TSN3	TSN2	TSN1	TSN0
Hardware RESET Configuration	0	1	1	0	0	0	0	0

Bit	Symbol	Name/Description
0-4	TSN04	Time Slot Side Network. These 5 bits indicate the time slot selected of 32 time slots corresponding to 64kb/s channel for transmitting and receiving. The H221 frame is transmitted and received in this channel.
5-7	MGN0-2	Maximum channel group side network. These 3 bits indicate the number of group of 4 B channels which constituites the multiplexes side network. **MGN2 MGN1 MGN0** 0 0 1 1 group of 4 Time Slots 0 1 0 2 group of 4 Time Slots 0 1 1 3 group of 4 Time Slots 1 0 0 4 group of 4 Time Slots 1 0 1 5 group of 4 Time Slots 1 1 0 6 group of 4 Time Slots 1 1 1 7 group of 4 Time Slots 0 0 0 8 group of 4 Time Slots Example TSAN is 61(h); TSN = 1, MGN = 3. The emitter and the receiver are connected onto the Time Slot 1 of multiplex which is constituited by 12 Time Slots.

Table 21: RBCR Register Definition (Address 1100).

Bit	7	6	5	4	3	2	1	0
(Read) Field	RF0	RB6	RB5	RB4	RB3	RB2	RB1	RB0

Bit	Symbol	Name/Description
0-6	RB0-6	Byte received. These 7 bits indicate the number of octet received (Modulo 80).
7	RF0	Frame Received. RF0 = Even frame RF0 = 1 Odd Frame.

Table 22: TDI1 Register Definition (Address 1101).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T81	T71	T61	T51	T41	T31	T21	T11
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T11	Subchannel 1 to be emitted comes from TDI1 pin.
1	T21	Subchannel 2 to be emitted comes from TDI1 pin.
2	T31	Subchannel 3 to be emitted comes from TDI1 pin.
3	T41	Subchannel 4 to be emitted comes from TDI1 pin.
4	T51	Subchannel 5 to be emitted comes from TDI1 pin.
5	T61	Subchannel 6 to be emitted comes from TDI1 pin.
6	T71	Subchannel 7 to be emitted comes from TDI1 pin.
7	T81	Subchannel 8 to be emitted comes from TDI1 pin.

Table 23: TDI2 Register Definition (Address 1110).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T82	T72	T62	T52	T42	T32	T22	T12
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T12	Subchannel 1 to be emitted comes from TDI2 pin.
1	T22	Subchannel 2 to be emitted comes from TDI2 pin.
2	T32	Subchannel 3 to be emitted comes from TDI2 pin.
3	T42	Subchannel 4 to be emitted comes from TDI2 pin.
4	T52	Subchannel 5 to be emitted comes from TDI2 pin.
5	T62	Subchannel 6 to be emitted comes from TDI2 pin.
6	T72	Subchannel 7 to be emitted comes from TDI2 pin.
7	T82	Subchannel 8 to be emitted comes from TDI2 pin.

Table 24: TDI3 Register Definition (Address 1111).

Bit	7	6	5	4	3	2	1	0
(Write) Field	T83	T73	T63	T53	T43	T33	T23	T13
Hardware RESET Configuration	0	0	0	0	0	0	0	0

Bit	Symbol	Name/Description
0	T13	Subchannel 1 to be emitted comes from TDI3 pin.
1	T23	Subchannel 2 to be emitted comes from TDI3 pin.
2	T33	Subchannel 3 to be emitted comes from TDI3 pin.
3	T43	Subchannel 4 to be emitted comes from TDI3 pin.
4	T53	Subchannel 5 to be emitted comes from TDI3 pin.
5	T63	Subchannel 6 to be emitted comes from TDI3 pin.
6	T73	Subchannel 7 to be emitted comes from TDI3 pin.
7	T83	Subchannel 8 to be emitted comes from TDI3 pin.

Table 25: Circuit Configuration.

	Input/Output	PROT = 0	PROT = 1
CONF = 0	Side Network	DCLR = 64kHz DCLT = 64kHz	One GCI channel: Data rate 256kb/s DCLR = DCLT = 512kHz
	Side Application	13 signals for external multiplexer	
CONF = 1	Side Network	DCLR = 64kHz DCLT = 64KHz FSCR = FSCT must be supplied	1 to 8 GCI channels Data Rate n x 256kb/s DCLR = DCLT = n x 512kHz ($1 \leq n \leq 8$) FSR = FSCT 1 B channel selected of 32
	Side Application	3 Input Multiplex 3 Output Multiplex 1 64kb/s selected of 32	

Figure 1: Circuit Interfaces.

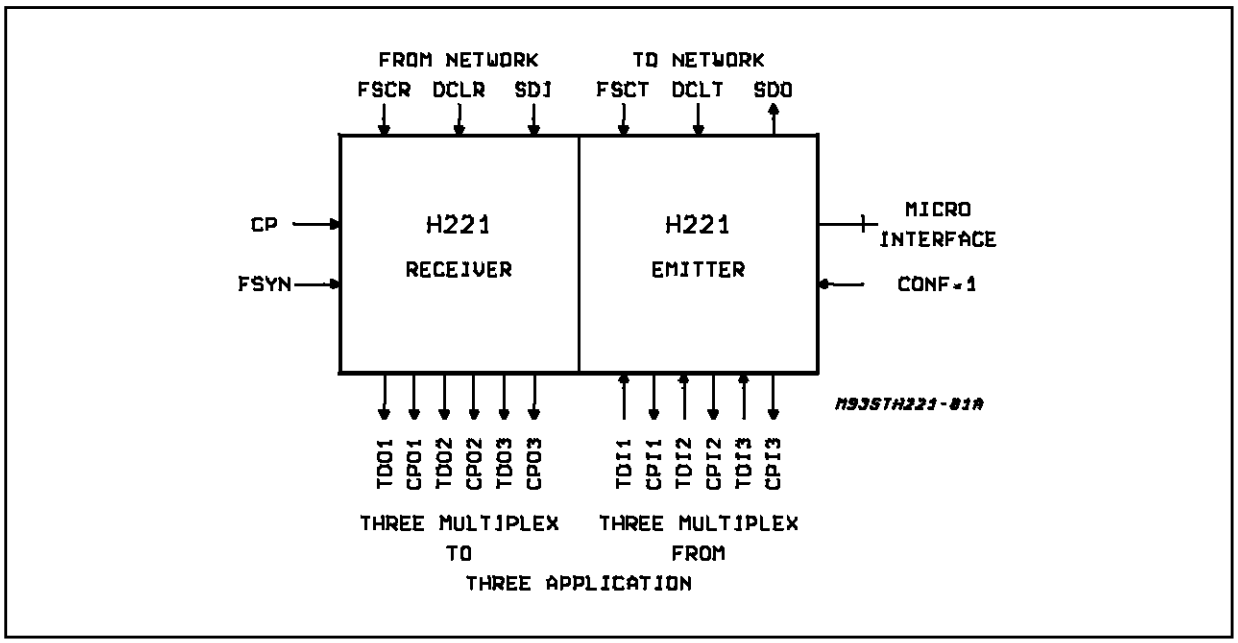


Figure 2: Video and Audio Terminal.

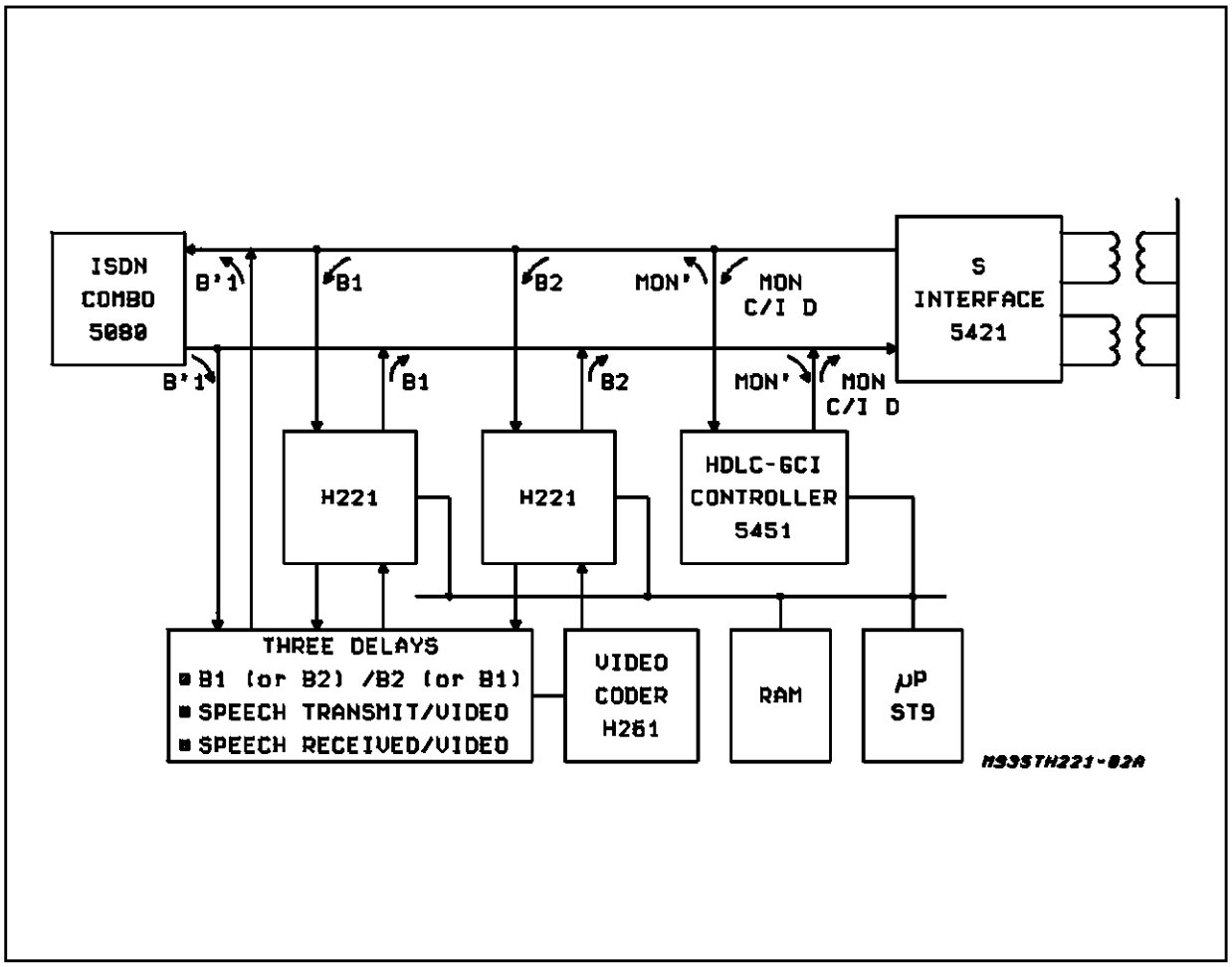


Table 24: Multiframe Structure.

	Submultiframe	Frame	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
MULTIFRAME	0	0	N1							
		1	0							
	1	2	N2							
		3	0							
	2	4	N3							
		5	1							
	3	6	N4	0	0	1	1	0	1	1
		7	0	1	A	E	C1	C2	C3	C4
	4	8	N5							
		9	1							
	5	10	L1							
		11	1							
	6	12	L2							
		13	L3							
	7	14	TEA							
		15	R							

Multiframe Synchronization: Bit 1 of frames 1, 3, 5, 7, 9, 11.
Multiframe number: N1, N2, N3, N4, N5.
Channel number: L1, L2, L3.
Terminal Equipment Alarm TEA, Bit reserved R.

Figure 3: H221 Multiframe.

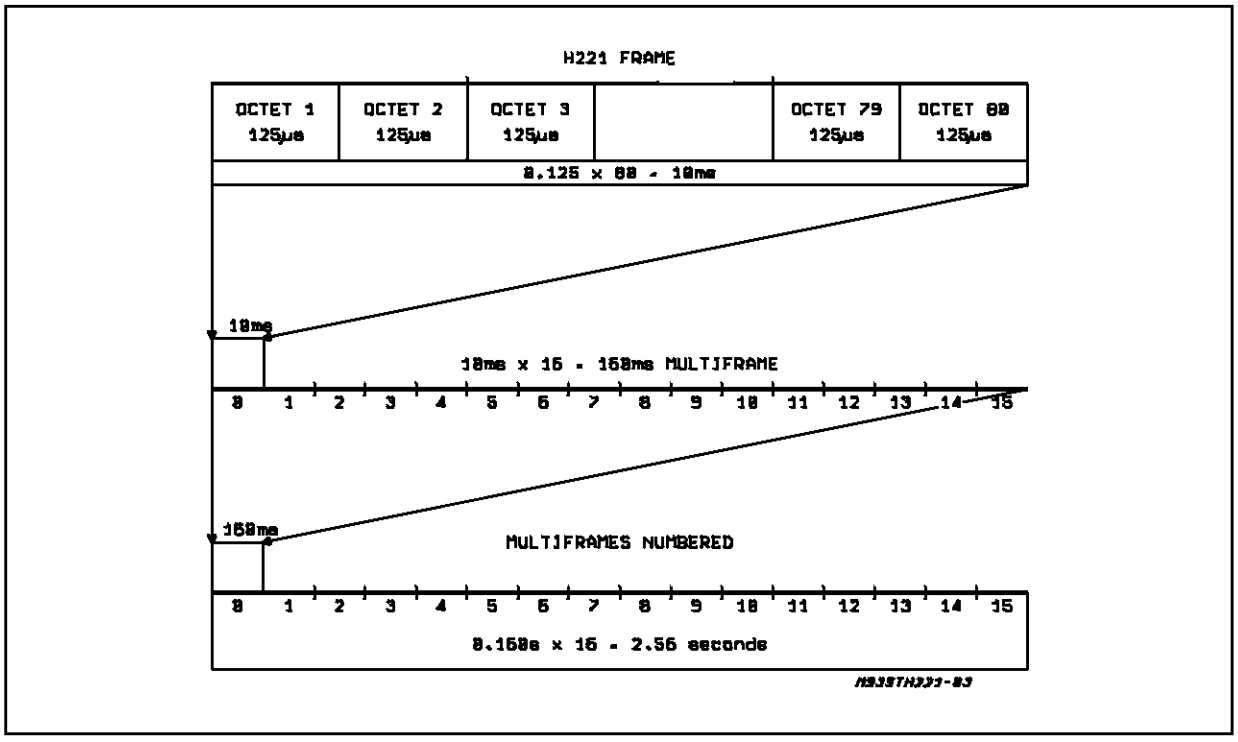
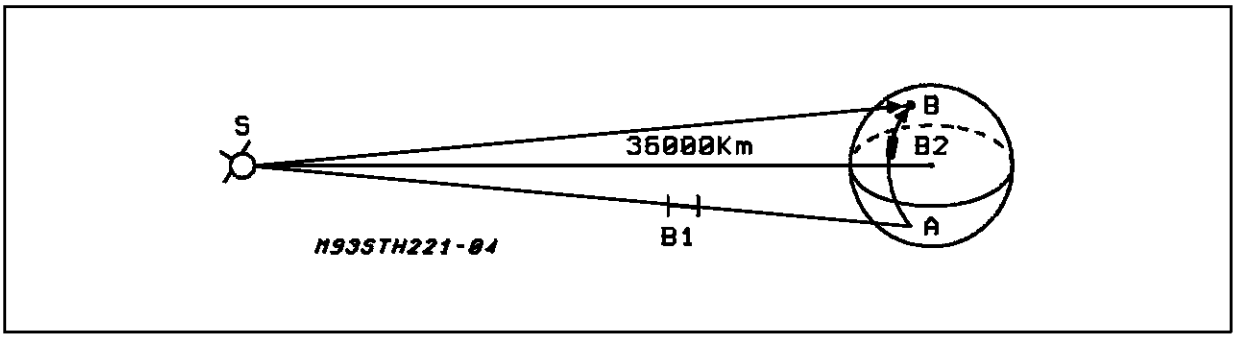


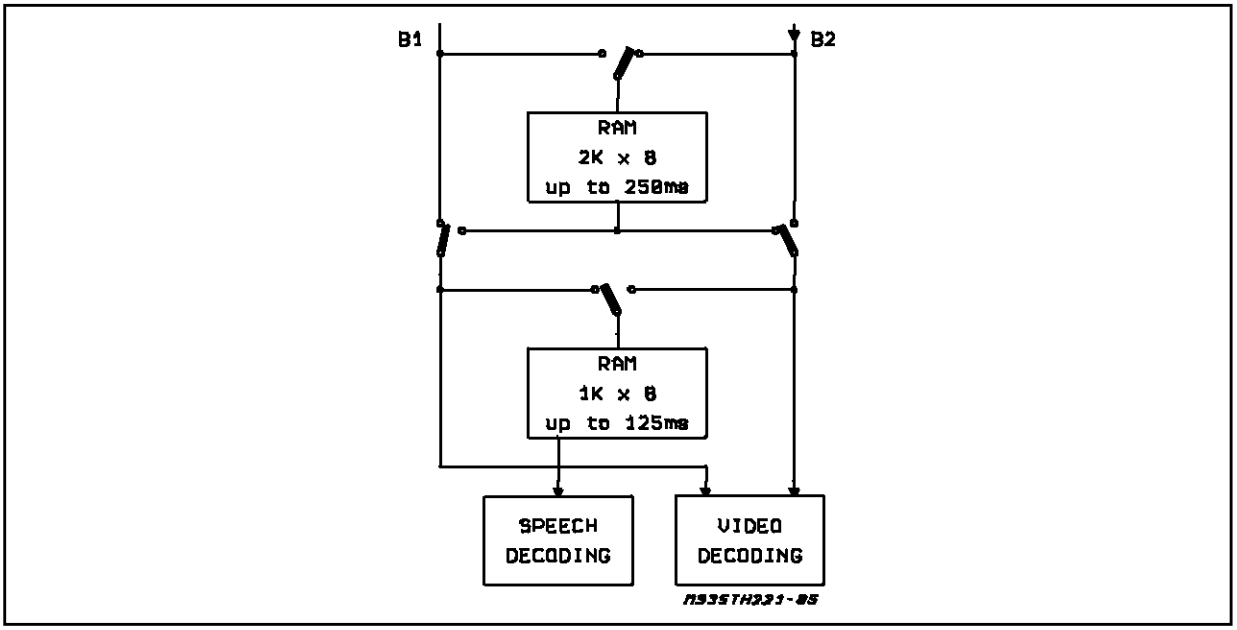
Figure 4: Possible Delays of B1 and B2 Channels.



B1 channel path ASB 300000Km/s Delay $\frac{3600 \cdot 2}{300000} = 0.240s$.

B2 channel path (AB) 5ms/Km (AB) = 6000Km Delay $6000 \cdot 5 = 30000\mu s$
Difference between B1 and B2: 240 - 30ms = 210ms

Figure 5: Terminal Receiving.



Assumptions for videophone terminal.

– The delay of B1 channel is greater than the delay of B2 channel (mp to 250 µs); B2 channel must be delayed.
– Video decoder is slower than the speech decoding up to 100ms.
– B1 is reserved to speech.
– B2 is reserved to video.

Figure 6: Two H.221 Frames Transmetting.

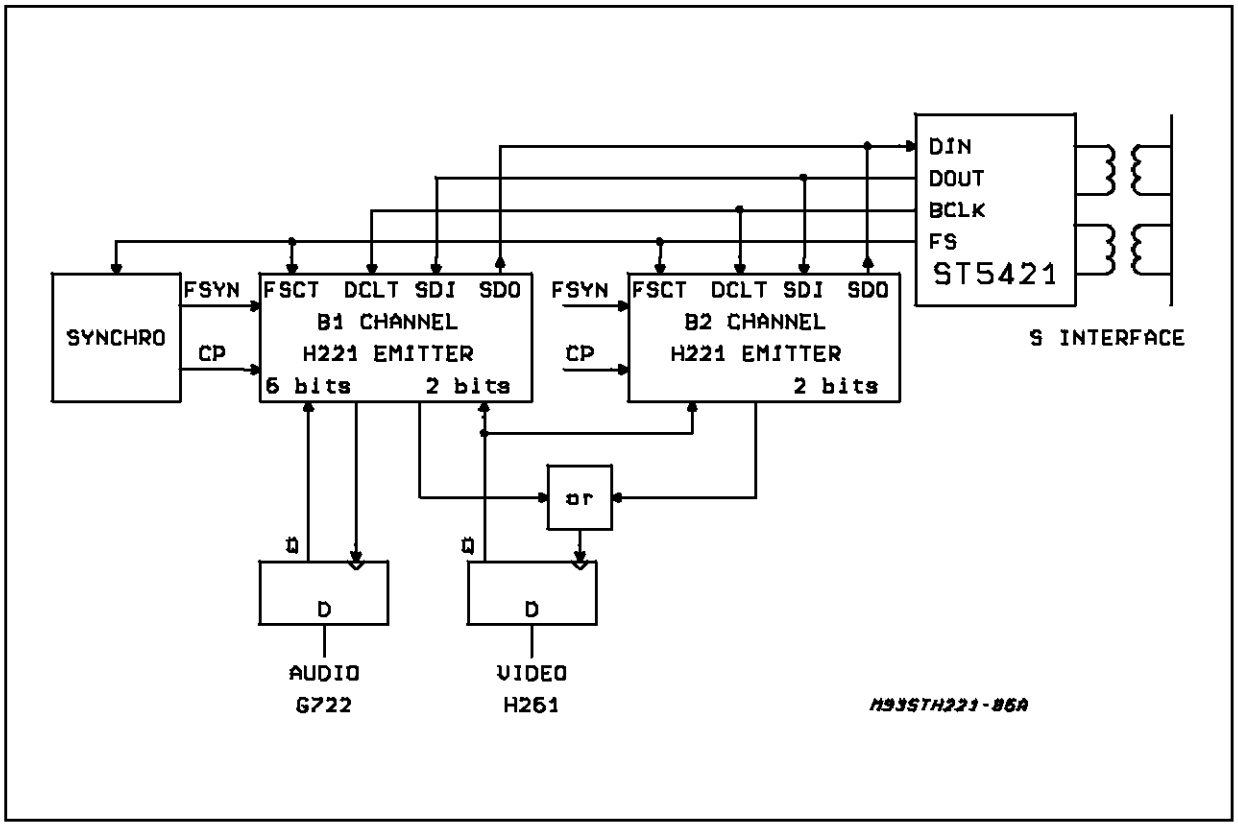


Figure 7: B1 channel is slower than B2 channel.

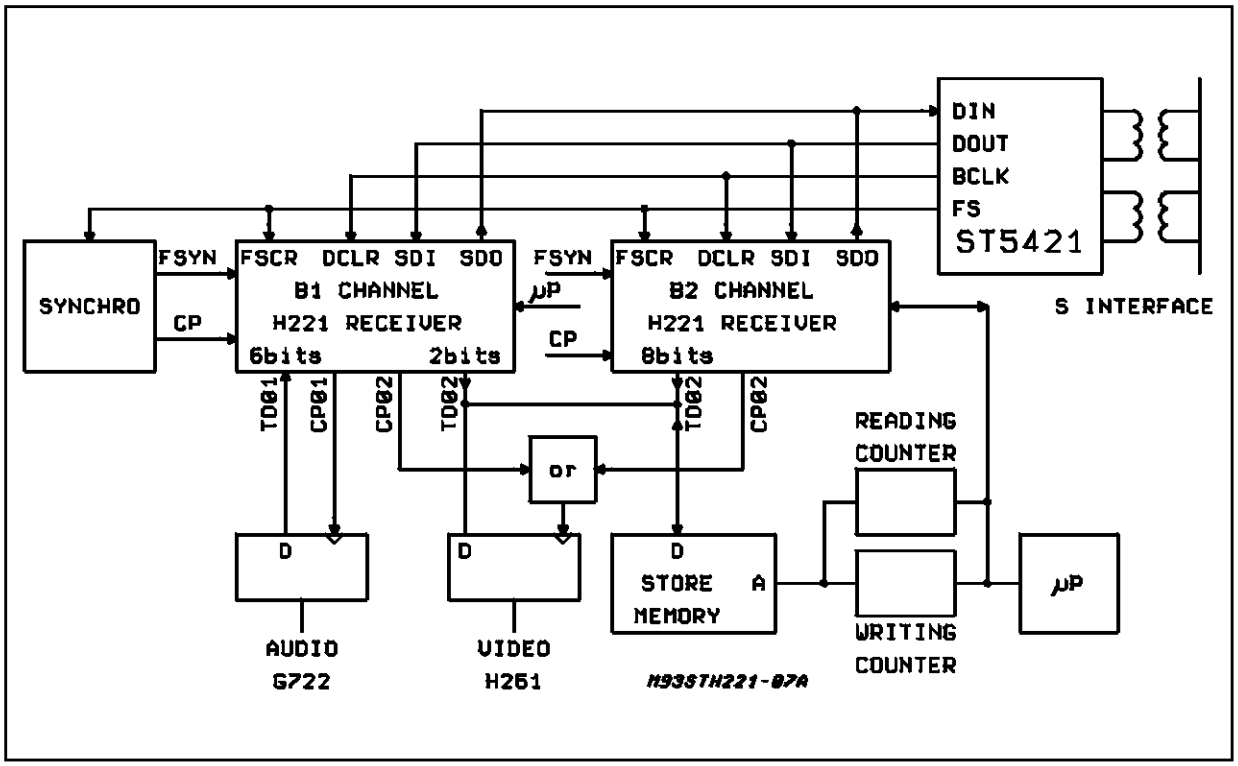


Figure 8: Application Interface Configuration can change every 20ms.

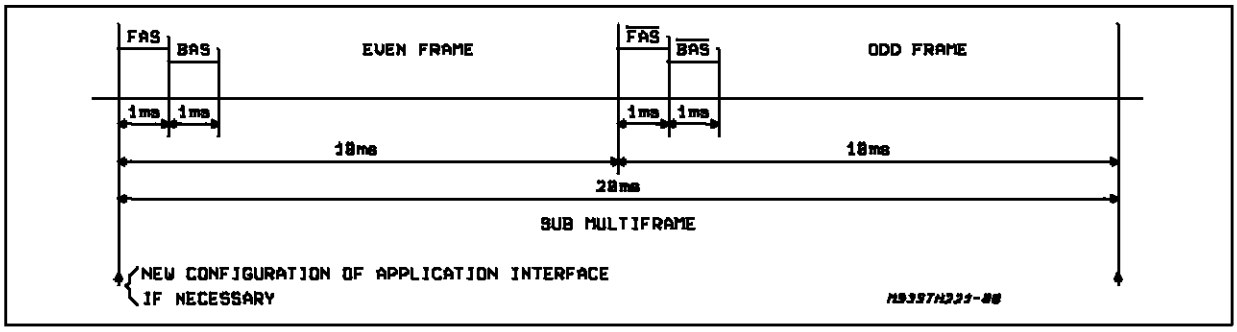


Figure 9: Sub multiframe received.

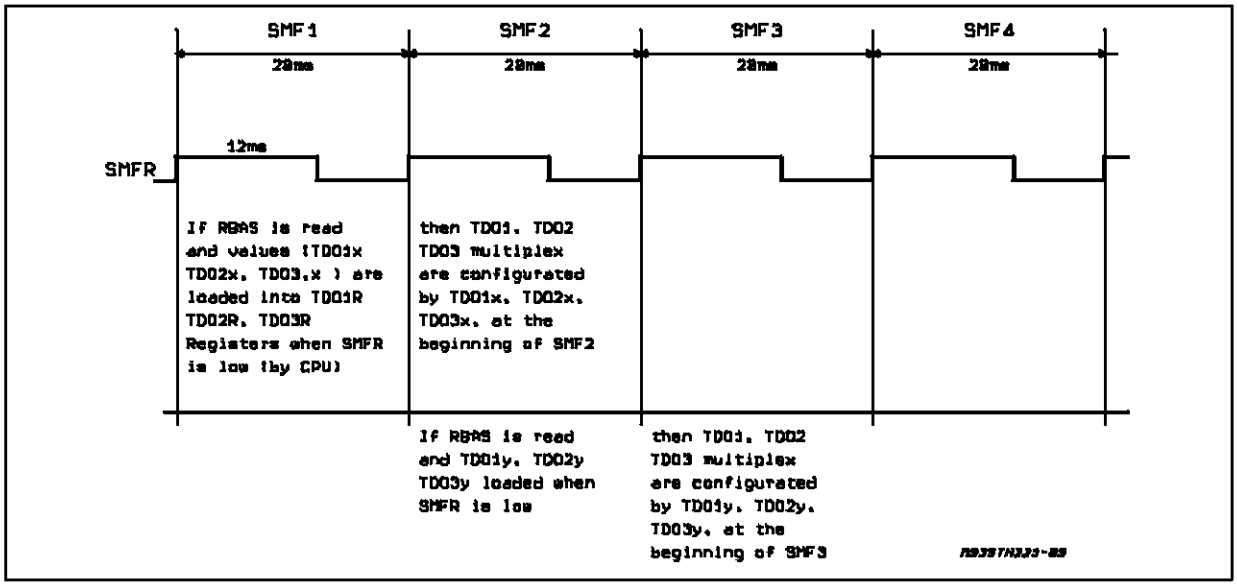


Figure 10: Sub multiframe emitted.

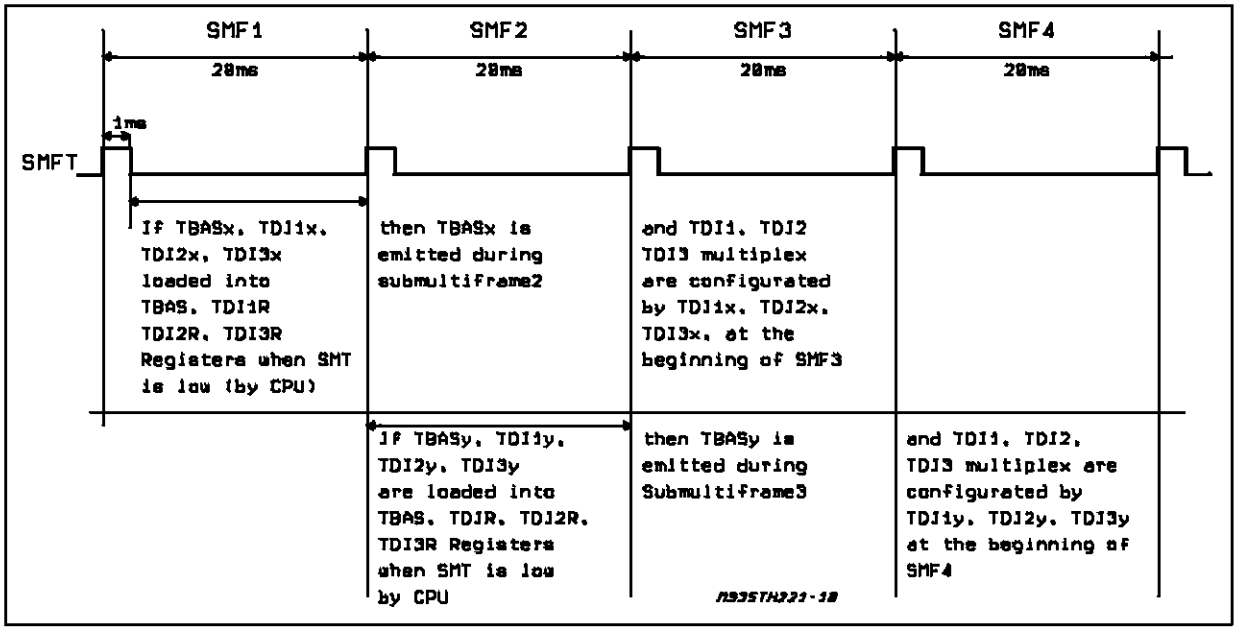


Figure 11: FSYN in comparison with FS when FSYN is different from FS.

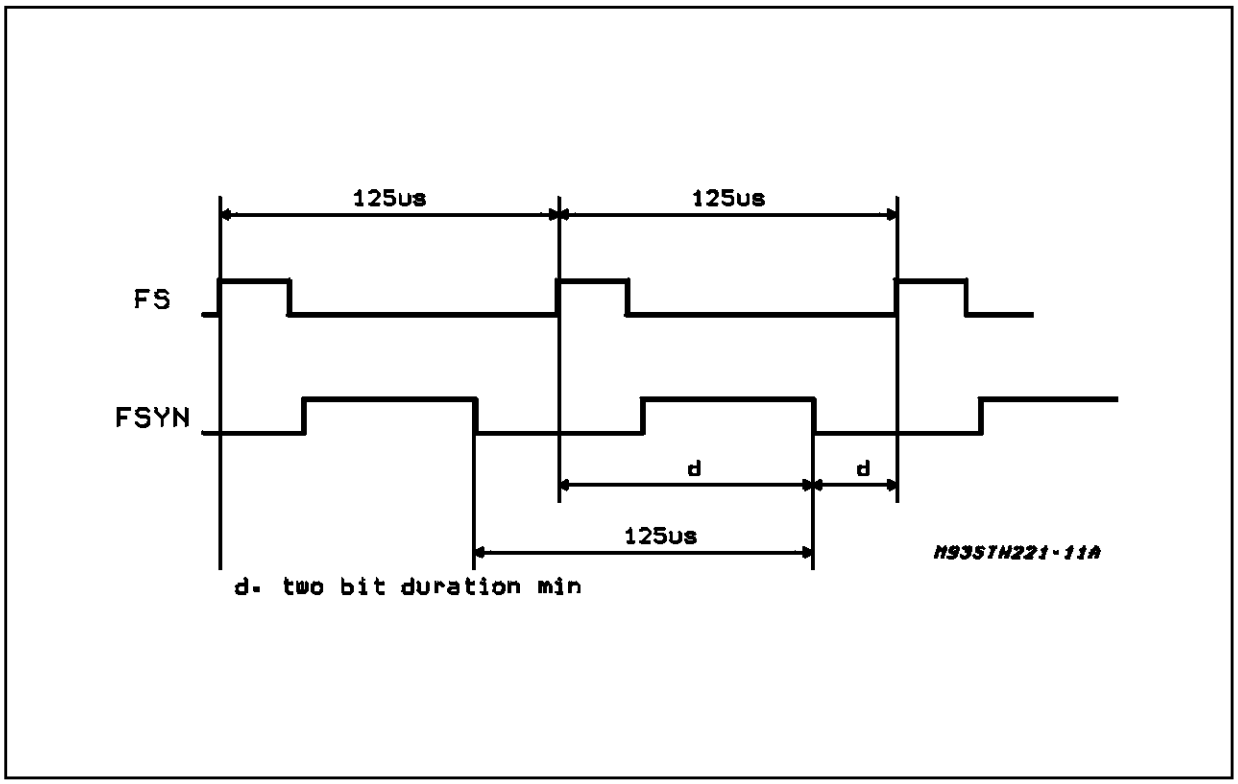
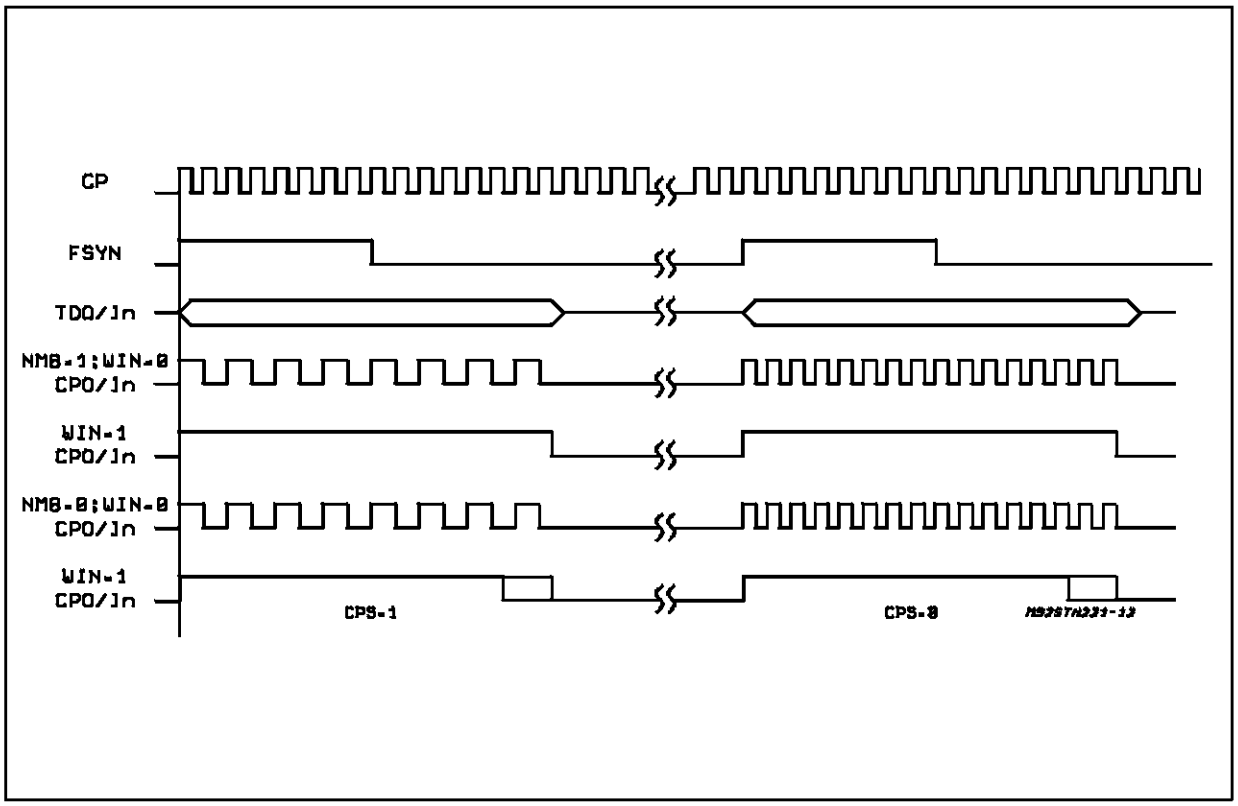


Figure 12: Application Interface.



TIMING CHARACTERISTICS (Preliminary)

Table 25: CPU Read and Write Timing.

Symbol	Description	Min.	Max.	Unit
t_{CTS}	CSN, CDN, RWN, BUS Set-Up Time	40	–	ns
t_{CTH}	CSN, CDN, RWN, BUS Hold Time	10	–	ns
t_{DTS}	DTACKN Valid Offset	–	20	ns
t_{DTH}	DTACKN Release	–	20	ns
t_{DSW}	DSN Width	40	–	ns
t_{DSS}	Data Valid Offset	–	20	ns
t_{DSH}	Data Release	–	20	ns

TIMING DIAGRAMS.

Figure 13: CPU Write Cycle

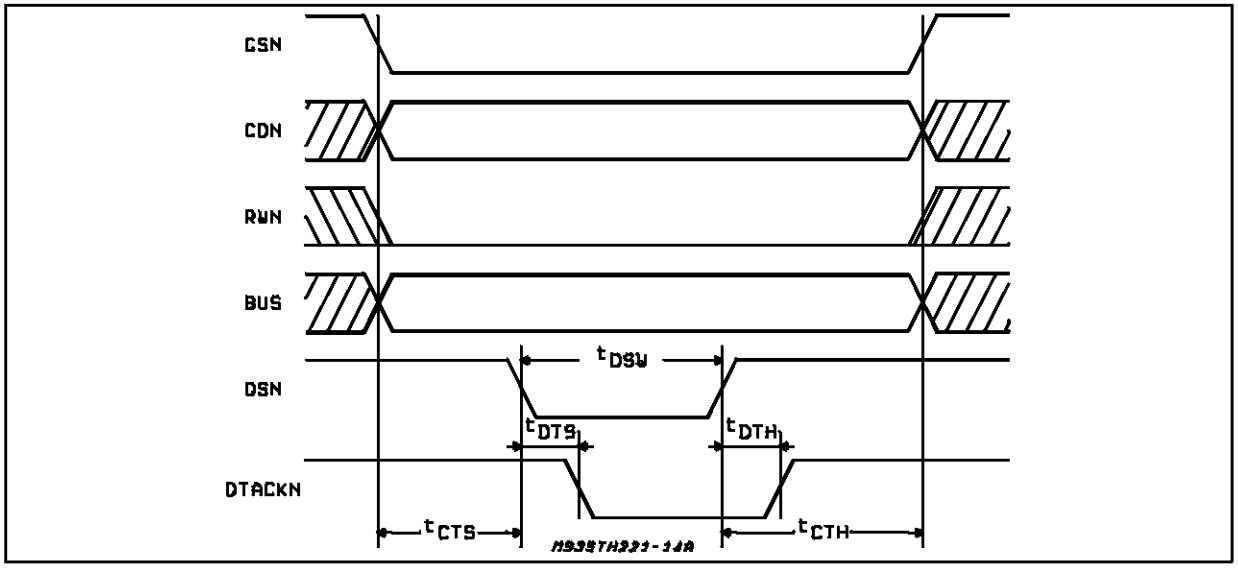


Figure 14: CPU Read Cycle

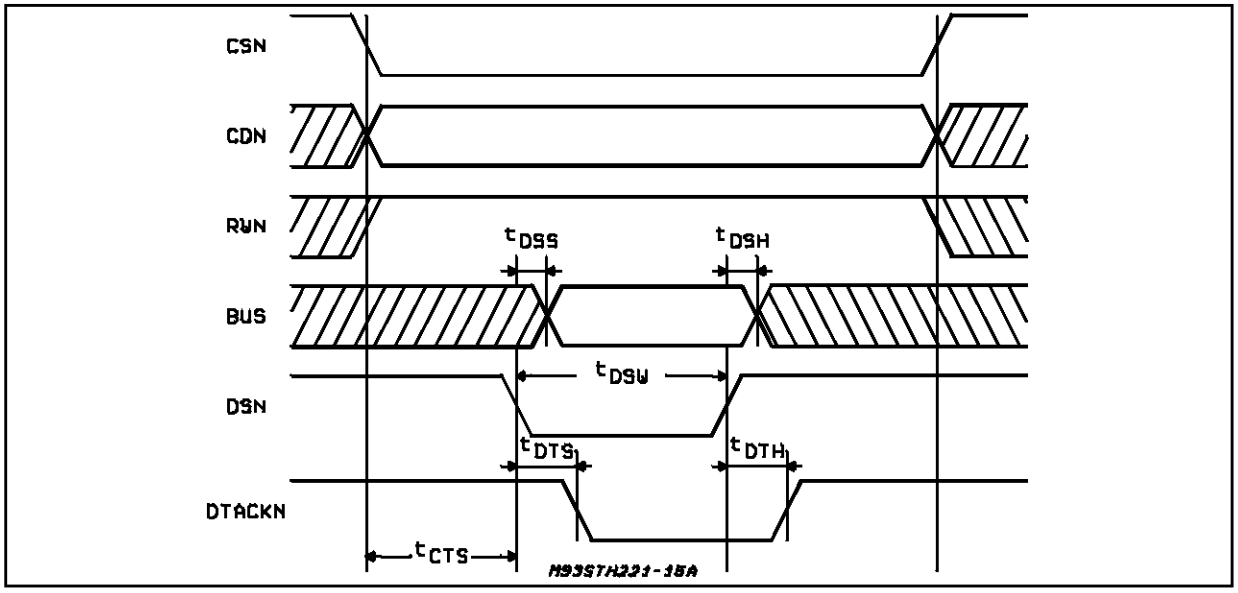


Figure 15: Transmitter Start Timing.

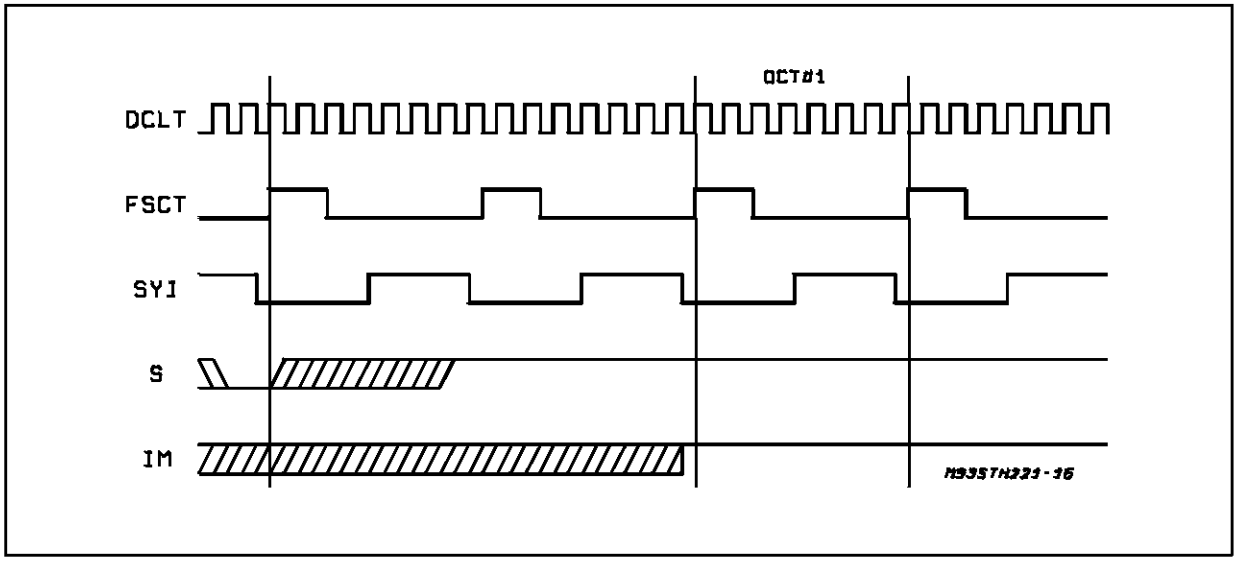


Table 26: Network Side Timing Specifications

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{HCF}	Hold Time DCLR/DCLT Transition to FSCR/FSCT Transition		0		ns
t_{RC}, t_{FC}	Rise and Fall Time: DCLR/DCLT			15	ns
t_{WCH}, t_{WCL}	DCL Width High and Low		60		ns
t_{SFC}	Set up Time FS High to DCL Low		70	DCL –50	ns
t_{DCD}	Delay Time DCL High to Data Valid	Load 150pF		80	ns
t_{DFD}	Delay Time FS High to Data Valid	Load 150pF		80	ns
t_{DCZ}	Delay Time DCL Low Data Invalid			120	ns
t_{SDC}	Set up Time Data Valid to DCL Low		30		ns
t_{HDC}	Hold Time DCL Low to Data Invalid		20		ns

Table 27: Application Side Timing Specifications

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{WCH}, t_{WCL}	CP width High and Low	CP = m · 128kHz $1 \leq m \leq 32$	60	–	ns
t_{RC}, t_{FC}	Rise and Fall Time CP		–	15	ns
t_{SFC}	Set Up Time FSYN High to CP Low		70	CP –50	ns
t_{DCDa}	Delay Time CP High to Data Valid	Load 150pF	–	70	ns
t_{DFDa}	Delay Time FSYN High to Data Valid	Load 150pF	–	90	ns
t_{DCZ}	Delay Time CP Low to Data Invalid		–	120	ns
t_{SDC}	Set Up Time Data Valid to CP Low		30	–	ns
t_{HDC}	Hold Time CP Low to Data Invalid		20	–	ns

Table 27: Application Side Timing Specifications (continued)

Symbol	Test Conditions	Parameters	Min.	Max.	Unit
t_{DCC}	Delay Time CP High to CPO1/3, CPI1/3 High		–	60	ns
t_{DCW}	Delay Time CP Low to window High and Low		–	80	ns
t_{DFC}	Delay Time FSYN High to CPO 1/3, CPI 1/3 High	First Clock Pulse of First Time Slot	–	80	ns
t_{DFW}	Delay Time FSYN High to window High	First Clock Pulse of First Time Slot	–	80	ns
t_{DDT}	Delay Time DCLT High to SFMT High and Low		–	80	ns
t_{DDR}	Delay Time DCLR High to SFMR High and Low		–	80	ns
t_{DDO}	Delay Time DCLR Low OB, OA, SYO, OM valid	CONF = 0	–	60	ns
t_{DDI}	Delay Time DCLT Low to IB, IA, SYI IM valid	CONF = 0	–	60	ns
t_{SDC}	Set Up Time Data Valid to CPI Low	CONF = 0	30	–	ns
t_{HDC}	Hold Time CPI Low to Data Invalid	CONF = 0	20	–	ns

Figure 16: Network Side Signals.

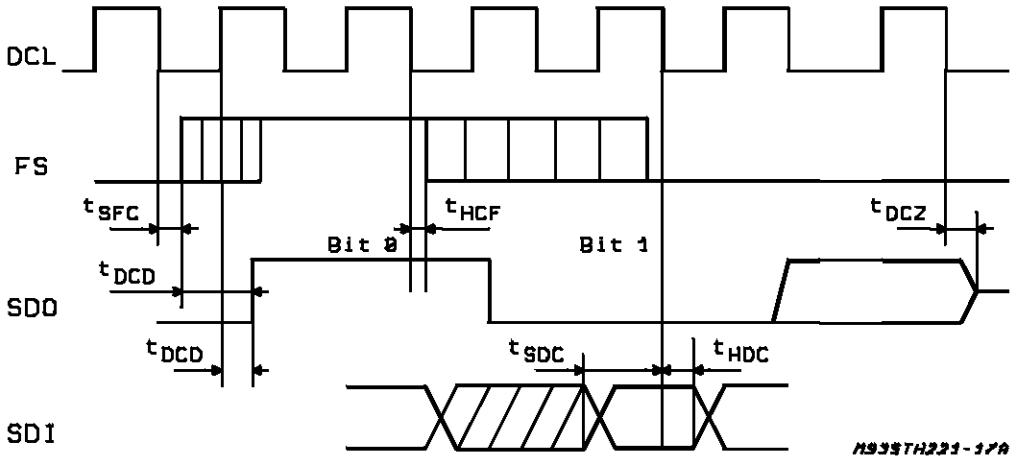
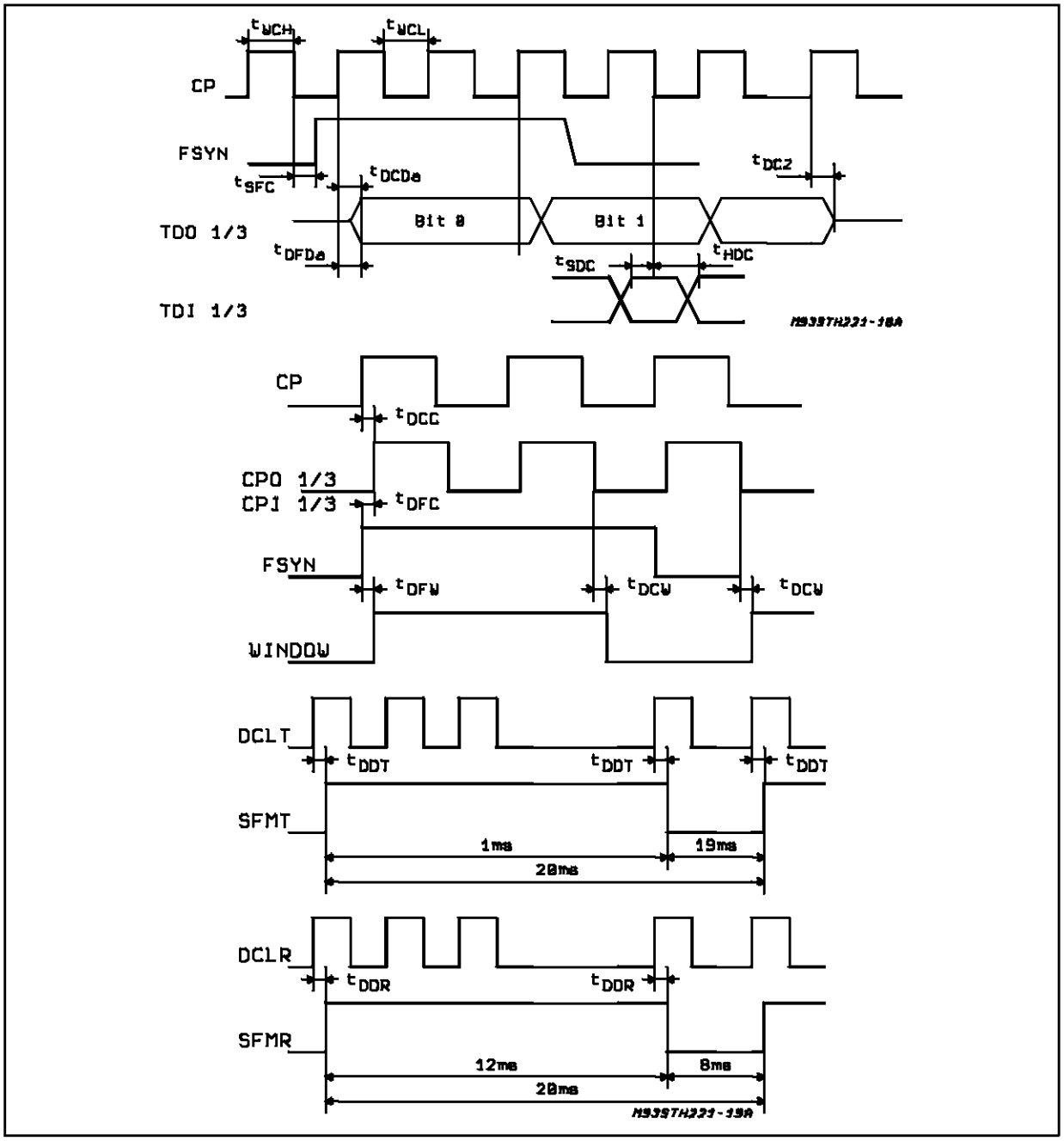


Figure 17: Application Side Signals.



PQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.30		0.45	0.0118		0.0177
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		12.00			0.472	
e		0.80			0.0315	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
K	0°(min.), 7°(max.)					
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063